Claims

[c1] 1. A circuit for monitoring defects in an integrated circuit, comprising:

a defect monitor comprising a nominally continuous conductor having a length and a multiplicity of conductor segments, each conductor segment having a length, at least a portion of the length of each conductor segment adjacent to a portion of the length of said nominally continuous conductor;

a first set of sense elements coupled to said nominally continuous conductor at locations along the length of said nominally continuous conductor located between conductor segments ;

a second set sense elements coupled to corresponding conductor segments of multiplicity of conductor segments; and

gates responsive to a control signal on select inputs of said gates to serially and electrically connect said conductor segments into a nominally electrically continuous conductive path based on a first logical value of said control signal and to electrically disconnect said conductor segments from one another based on a second logical value of said control signal.

[c2] 2. The circuit of claim 1, wherein:
said first set of sense elements comprise a first set of latches and said second set of sense elements comprise a second set of latches, said first set of latches and said second set of latches comprise a scan chain having a scan input and a scan output.

[c3] 3. The circuit of claim 2, wherein:
said scan chain further includes a setup latch, said first and second logical values of said control signal based on logical values latched by said setup latch.

[c4] 4. The circuit of claim 2, wherein:
(a) in the event of an open fault in said nominally continuous conductor, latches of said first set of latches that are coupled between a location of said open fault and said scan output are adapted to switch from an initial state to a fault state;
(b) in the event of an open fault in a particular conductor segment of said multiplicity of conductor segments, latches of said second set of latches that a coupled between a location of said open fault and said scan output are adapted to switch from an initial state to a fault state; and
(c) in the event of a short fault between said nominally continuous conductor and said particular conductor seg-

ment of said multiplicity of conductor segments, a corresponding latch of said second set of latches that is coupled to said particular conductor segment of said multiplicity of conductor segments is adapted to switch from said initial state to said fault state.

[c5] 5. The circuit of claim 2, wherein:
said first set of latches are coupled in series from a first latch to a last latch and said second set of latches are coupled in series from a first latch to a last latch;
said first latch of said first set of latches adapted to set a first voltage level on said nominally continuous conductor to a first voltage value in the event of a logical one on an output port of a first latch of said first set of latches;
said first latch of said first set of latches adapted to set said first voltage level on said nominally continuous conductor to a second voltage value in the event of a logical zero on said output port of said first latch of said first set of latches;
said first latch of said second set of latches adapted to set a second voltage level on said conductor segments to said first voltage value in the event of a logical one on an output port of a first latch of said second set of latches; and
said first latch of said second set of latches adapted to set said second voltage level on said conductor seg-

ments to said second voltage value in the event of a logical zero on said output port of said first latch of said second set of latches.

[c6] 6. The circuit of claim 5, further including:
providing one or more first devices adapted to apply said second voltage value to any portion of said nominally continuous conductor that becomes electrically disconnected from said output port of said first latch of said first set of latches; and
one or more second devices adapted to apply said second voltage value to any conductor segment that becomes electrically disconnected from said output port of said first latch of said second set of latches.

[c7] 7. The circuit of claim 6, wherein:
said first and second devices are independently selected from the group consisting of diodes, floating gate diodes, transistors, pass gates, transmission gates, other switching devices or combinations thereof, and wherein said gates are transmission gates.

[c8] 8. The circuit of claim 2, wherein:
said scan chain is a section of a larger scan chain, other sections of said larger scan chain adapted to test functional circuits formed in said integrated circuit.

[c9] 9. The circuit of claim 1, wherein:
said a spacing between said nominally continuous conductor and a portion of the length of any particular conductor segment of said multiplicity of conductor segments is based on a size of said defects to be detected.

[c10] 10. A method for monitoring defects in an integrated circuit, comprising:
providing a defect monitor comprising a nominally continuous conductor having a length and a multiplicity of conductor segments, each conductor segment having a length, at least a portion of the length of each conductor segment adjacent to a portion of the length of said nominally continuous conductor;
providing a first set of sense elements;
coupling said first set of sense elements to said nominally continuous conductor at locations along the length of said nominally continuous conductor located between conductor segments;
providing a second set sense elements;
coupling said second set sense elements to corresponding conductor segments of multiplicity of conductor segments; and
providing gates responsive to a control signal on select inputs of said gates to serially and electrically connect said conductor segments into a nominally electrically

continuous conductive path based on a first logical value of said control signal and to electrically disconnect said conductor segments from one another based on a second logical value of said control signal.

[c11] 11. The method of claim 10, wherein:
said first set of sense elements comprise a first set of latches and said second set of sense elements comprise a second set latches, said first set of latches and said second set of latches comprise a scan chain having a scan input and a scan output.

[c12] 12. The method of claim 11, wherein:
said scan chain further includes a setup latch, said first and second logical values of said control signal based on logical values latched by said setup latch.

[c13] 13. The method of claim 11, wherein:
(a) in the event of an open fault in said nominally continuous conductor, switching latches of said first set of latches that are coupled between a location of said open fault and said scan output from an initial state to a fault state;
(b) in the event of an open fault in a particular conductor segment of said multiplicity of conductor segments, switching latches of said second set of latches that a coupled between a location of said open fault and said

scan output from an initial state to a fault state; and
(c) in the event of a short fault between said nominally continuous conductor and said particular conductor segment of said multiplicity of conductor segments, switching a corresponding latch of said second set of latches that is coupled to said particular conductor segment of said multiplicity of conductor segments from said initial state to said fault state.

[c14] 14. The method of claim 11, wherein:
said first set of latches are coupled in series from a first latch to a last latch and said second set of latches are coupled in series from a first latch to a last latch;
said first latch of said first set of latches adapted to set a first voltage level on said nominally continuous conductor to a first voltage value in the event of a logical one on an output port of a first latch of said first set of latches;
said first latch of said first set of latches adapted to set said first voltage level on said nominally continuous conductor to a second voltage value in the event of a logical zero on said output port of said first latch of said first set of latches;
said first latch of said second set of latches adapted to set a second voltage level on said conductor segments to said first voltage value in the event of a logical one on an output port of a first latch of said second set of latches;

and
said first latch of said second set of latches adapted to set said second voltage level on said conductor segments to said second voltage value in the event of a logical zero on said output port of said first latch of said second set of latches.

[c15] 15. The method of claim 14, further including:
providing one or more first devices for applying said second voltage value to any portion of said nominally continuous conductor that becomes electrically disconnected from said output port of said first latch of said first set of latches; and
providing one or more second devices for applying said second voltage value to any conductor segment that becomes electrically disconnected from said output port of said first latch of said second set of latches.

[c16] 16. The method of claim 15, wherein:
said first and second devices are independently selected from the group consisting of diodes, floating gate diodes, transistors, pass gates, transmission gates, other switching devices or combinations thereof, and wherein said gates are transmission gates.

[c17] 17. The method of claim 11, wherein:
said scan chain is a section of a larger scan chain, other

sections of said larger scan chain adapted to test functional circuits formed in said integrated circuit.

[c18] 18. The method of claim 10, wherein a spacing between said nominally continuous conductor and a portion of the length of any particular conductor segment of said multiplicity of conductor segments is based on a size of said defects to be detected.

[c19] 19. A circuit for monitoring defects in an integrated circuit , comprising:
a scan chain comprising a scan input, a multiplicity of latches coupled in series from a first latch to a second latch and a scan output;
a multiplicity of electrically conductive defect monitor structures, each defect monitor structure coupled between different adjacent latches of said scan chain, an input of each defect monitor structure coupled to an output of a previous latch of said scan chain and an output of each defect monitor structure coupled to an input of an immediately subsequent latch of said scan chain; and
said scan input coupled to an input of said first latch in said scan chain and said scan output coupled to an output of said last latch in said scan chain.

[c20] 20. The circuit of claim 19, wherein said scan chain in-

cludes additional circuit elements interconnected to said multiplicity of latches to allow determination of particular latch or latches at which stuck at faults have occurred.

[c21] 21. The circuit of claim 19, further including:
a multiplicity of XOR gates coupled in series from a first XOR gate to a last XOR gate, each XOR gate coupled between one latch of said scan chain and one defect monitor structure adjacent to said one latch, a first input of each XOR gate coupled to the output of said one defect monitor structure and an output of each XOR gate couple to the input of said one latch of said scan chain; and
a second input of each XOR gate coupled to the first input of a previous XOR gate except a second input of said first XOR gate is coupled to said scan input.

[c22] 22. The circuit of claim 19, further including:
a multiplicity of XOR gates coupled in series from a first XOR gate to a second XOR gate, an output of each XOR gate coupled to an input of one latch of said scan chain and a first input each XOR coupled to the output of one defect monitor structure adjacent to said one latch except a first input of said first XOR gate is coupled to said scan input; and
a second input of each XOR gate coupled to a detect/diagnosis signal.

[c23] 23. The circuit of claim 19, wherein said defect monitor structures are via chains.

[c24] 24. The circuit of claim 19, wherein groups of one or more of said defect monitor structures comprise different design treatment circuits of a designed experiment, each design treatment circuit comprised of a different combination of integrated circuit process parameters, design parameters, performance parameter or combinations thereof.

[c25] 25. A method for monitoring defects in an integrated circuit , comprising:
providing a scan chain comprising a scan input, a multiplicity of latches coupled in series from a first latch to a last latch and a scan output;
providing a multiplicity of electrically conductive defect monitor structures, each defect monitor structure coupled between different adjacent latches of said scan chain, an input of each defect monitor structure coupled to an output of a previous latch of said scan chain and an output of each defect monitor structure coupled to an input of an immediately subsequent latch of said scan chain; and
said scan input coupled to an input of said first latch in said scan chain and said scan output coupled to an out-

put of said last latch in said scan chain.

[c26] 26. The method of claim 15, wherein said scan chain includes additional circuit elements interconnected to said multiplicity of latches to allow determination of particular latch or latches at which stuck at faults have occurred.

[c27] 27. The method of claim 25, further including:
providing a multiplicity of XOR gates coupled in series from a first XOR gate to a last XOR gate, each XOR gate coupled between one latch of said scan chain and one defect monitor structure adjacent to said one latch, a first input of each XOR gate coupled to the output of said one defect monitor structure and an output of each XOR gate couple to the input of said one latch of said scan chain; and
a second input of each XOR gate coupled to the first input of a previous XOR gate except a second input of said first XOR gate is coupled to said scan input.

[c28] 28. The method of claim 25, further including:
providing a multiplicity of XOR gates coupled in series from a first XOR gate to a last XOR gate, an output of each XOR gate coupled to an input of one latch of said scan chain and a first input each XOR coupled to the output of one defect monitor structure adjacent to said

one latch except a first input of said first XOR gate is coupled to said scan input; and
a second input of each XOR gate coupled to a detect/diagnosis signal.

[c29] 29. The method of claim 25, wherein said defect monitor structures are via chains.

[c30] 30. The method of claim 25, wherein groups of one or more of said defect monitor structures comprise different design treatment circuits of a designed experiment, each design treatment circuit comprised of a different combination of integrated circuit process parameters, design parameters, performance parameter or combinations thereof.